REMARKS

Claims 1, 3, 4, 7, 8, 11 – 15, and 17 – 21 are pending and at issue. Claims 2, 5, 6, 9, 10 and 16 have been canceled. Claims 1, 2, 4, 5, 7 – 9, 13, and 19 – 21 stand rejected under 35 U.S.C. 102(e) based on Anddreasson. Claims 3 and 10 – 12 stand rejected under 35 U.S.C. 103(a) based on Andreasson. Claims 7, 14, 15, 17, and 18 stand rejected under 35 U.S.C. 112, second paragraph. Of these claims, independent claim 14 and dependent claims 15, 17, and 18 have not been rejected on prior art grounds and therefore are considered to recite allowable subject matter. In light of the following remarks and accompanied by the above amendments, applicant respectfully traverses the rejections.

1. Rejections under 35 U.S.C. 112

The dependency typographical errors of claims 7 and 16 have been corrected by amendment above. These rejections are traversed.

Applicant separately traverses the rejection of claim 14. Contrary to the examiner's suggestion, the cited "determining" recitation is definite. The method states that a frequency count of the identified load miss memory addresses is maintained. The method then determines if any memory region includes a threshold number of these load miss memory addresses, as each load miss memory address can correspond to a different memory region in the heap. The examiner asks whether the claim language is met by a single threshold or many thresholds, for example, one for each memory region. Applicant responds by pointing to the plain language of the claim. The claim recites determining whether any of a plurality of memory regions have a threshold value of load miss memory addresses. While the written description is not limiting, it is illuminating in this regard. Paragraphs [0036] and [0037] discuss example implementations of a system capable of performing a method as recited in claim 14. That is, in some examples, a frequency count is maintained for each memory region and thus may be used to determine if a threshold number of load misses have occurred. Yet, in others the system, delinquent regions may be identified by identifying which memory regions have a certain percentage (e.g., 90%) of the total number of cache misses, DTLB misses, or the like. See, e.g., [0036] and [0037].

The examiner's suggested amendment to claim 14 would appear to exclude examples discussed in the written description and either way would not speak to the single versus multiple threshold question.

In any event, applicant respectfully asserts that claim 14 is definite. The rejection under 35. U.S.C. §112 is traversed and reconsideration requested. In fact, given that claim 14 has only been rejected based on this lone rejection, which has now been traversed, claim 14 is implicitly in condition for immediate allowance, as the examiner has levied no prior art rejection of the claim.

Thus, independent claim 14 and claims 15, 17 and 18 depending therefrom are in condition for immediate allowance.

2. Rejections under 35 U.S.C. 102/103

Turning to the remaining claims, based on the response to arguments portion of the office action it appears that a single issue remains: whether Andreasson's use of garbage collection on fragmented drive sectors is akin to determining a delinquent region and performing memory optimization on that region.

As applicant previously noted, Andreasson's garbage collection system is different than that claimed, as Andreasson is not directed toward the identification of or the correction of delinquent regions. Andreasson does discuss various garbage collection control techniques—e.g., reference counting collectors, mark-and-sweep tracing collectors, stop-and copy collectors, mark-and-compact collectors, generational collectors, incremental collectors, concurrent collectors, parallel collectors, and mostly-concurrent garbage collection. See, e.g., Adreasson 9:41 – 14:8. But Andreasson does not discuss the identification of a delinquent memory region or initiating garbage collection in a region identified as delinquent. The only citation offered by the office action as teaching an identification of "delinquent regions" is the discussion spanning columns 19 and 20 and pertaining to using the amount of fragmentation of a volume to affect garbage collection. There is nothing in Andreasson that links this fragmentation determination to identifying a memory region as delinquent.

The examiner responds that fragmentation is a form of delinquency, yet applicant previously noted, fragmentation does not necessarily or inherently mean that a region is delinquent, as fragmentation often occurs during normal memory heap operation and thread allocation. While applicant appreciates the examiner's comments in paragraph 2 of the office action, applicant notes that the such comments do not address the numerous examples of delinquency provided in the application. For example, the examiner cites to Berry et al. as teaching identifying cache misses, but Berry et al. does not identify cache misses for the purpose of determining that a memory region is delinquent or even fragmented, as would have to be the case to support the obviousness rejection of claim 3. Instead, Berry et al. uses measured time indicators such as "cycles, cache misses, microseconds, milliseconds, etc." as part of a trace record feature to profile code. The Berry et al. system uses trace record generation over different periods of time to compute "calibration values to be used to compensate for the instrumentation overhead introduced by the profiling process." Col. 23, ll. 31-34. These cache misses then are simply used to represent the amount of time required to generate trace records, which are then used to profile code execution. See, Abstract. In fact, the portion of Berry et al. at column 1 cited in the office action, makes clear that Berry et al. is directed to profiling code, not assessing or determining if a physical memory region is not performing. In other words, whereas the present application describes examples of using cache misses and other performance data metrics to identify physical regions of a memory heap as delinquent, the office action fails to point to any recognition of such in Andreasson, Berry et al., or any art of record.

In any event, to address the rejections and expedite allowance, applicant has amended various independent claims. Claim 1 for example has been amended to include the subject matter of previous dependent claims 5, 9, and 10 (now canceled).

> 1. (Previously presented) An article comprising a machine-accessible medium having stored thereon instructions that, when executed by a machine, cause the machine to:
>
> obtain, from a performance monitor, performance data for a memory heap having a plurality of memory regions;
>
> based on the performance data, determine if at least one of the plurality memory regions is a delinquent region, wherein said determining includes instructions that when executed cause the machine to count the number of occurrences of the

> performance data and to compare the count of the number of occurrences of the performance data to a threshold value, wherein if the count has reached the threshold value, a delinquent region is determined to exist; ~~and~~
>
> in response to a determination that at least one of the plurality of memory regions is a delinquent region, execute a memory management routine to optimize that region of the memory heap by executing a garbage collection routine on at least one delinquent region, the garbage collection routine re-arranging the plurality of memory regions stored in the memory heap to optimize the memory heap; and
>
> execute a secondary memory management routine on at least one non-delinquent region, wherein the secondary memory management routine is different than the memory management routine.

Thus, claim 1 now recites that the delinquent region is determined to exist when a threshold value of occurrences of a performance data have occurred. For example, if a threshold number of the cache misses occur in a particular memory region then that region may be identified as delinquent. In other examples, any memory region that experiences a threshold number of occurrences of the performance data may be identified as delinquent. Claim 1 also recites that the system is able to execute one type of memory management routine on an identified delinquent region while executing another type of memory management routine on non-delinquent regions, a recognition that the system may not only identify delinquent regions from non-delinquent regions, but differentiate in how those regions are addressed.

In fact, this ability to both identify delinquent regions and differentiate them from the treatment of other memory regions is wholly absent from Andreasson. In rejecting prior dependent claim 5, the office action pointed to Andreasson's ability to variously apply different garbage collection routines. The office action cites to nothing actually in Andreasson that shows applying different garbage collection routines to different sections. Yet, even if Andreasson would apply different routines to different sections such would not be based on the Andreasson system determining that one region is delinquent (e.g., having a threshold number of occurrences of a performance data) while another region is not. In fact, the examiner's suggestion that any fragmentation is a form of delinquency and fragmentation

triggers garbage collection belies any suggestion that Andreasson could distinguish between delinquent and non-delinquent and selectively apply memory management routines to each.

Simply put, nowhere does Andreasson or any other art of record teach the combination of using the number of occurrences of a performance data to identify delinquent from non-delinquent regions with an ability selectively apply different memory management routines based on such a determination.

For the foregoing reasons, the rejection of claim 1 is traversed, as are the rejections of the claims depending therefrom. Reconsideration is respectfully requested.

The only remaining independent claim is claim 19. Applicant amends claim 19 by amendment above, and respectfully asserts that claim 19 is in condition for immediate allowance in light of the foregoing remarks.

> 19. (Currently amended) A system comprising:
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> hardware to monitor performance of a memory heap and to compile performance data on memory regions within the memory heap, wherein the hardware is able to determine if any of the memory regions are delinquent regions based on the compiled performance data and wherein the hardware has a memory manager for optimizing the delinquent regions by re-arranging memory regions in the memory heap in response to a determination of at least one delinquent ~~member~~ memory region, wherein a delinquent memory region is one that has at least a threshold number of occurrences of a memory performance event, and a non-delinquent region is one that has less than a threshold number of occurrences of a memory performance event; and
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> a memory manager in the form of a garbage collector for optimizing the delinquent regions using a first garbage collection routine and for optimizing non-delinquent regions using a second garbage collection routine different than the first garbage collection routine.

Namely, claim 19 recites a system that not only has hardware to determine if a memory region is delinquent, but that also has a memory manager for optimizing delinquent regions using a first garbage collection routine and for optimizing non-delinquent regions using a second, different garbage collection routine.

For at least the foregoing reasons outlining distinctions between the present application and Andreasson, the rejections of each of the pending claims are traversed.

In view of the above amendment, applicant believes the pending claims 1-5, 7-15, and 17-21 are in condition for allowance.

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Respectfully submitted,

By _____

Paul B. Stephens
Registration No.: 47,970
MARSHALL, GERSTEIN & BORUN LLP
233 S. Wacker Drive, Suite 6300
Sears Tower
Chicago, Illinois 60606-6357
(312) 474-6300
Attorney for Applicant